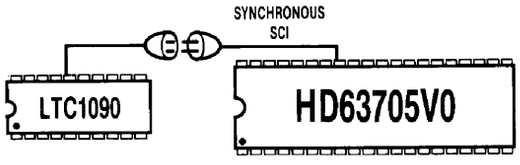
Interfacing the LTC1090 to the HD63705V0 MCU



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Introduction

This application note describes an interface between the LTC1090 10-bit data acquisition system and the Hitachi 63705 microcomputer. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 63705 in 45μs. Configuration of the LTC1090 and the 63705 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The Hitachi Serial Communication Interface (SCI) is a synchronous, full duplex, serial port built into the 63705 that allows the user to construct a simple communication path to the LTC1090. SCI provides clock, transmit and receive lines that are compatible with the LTC1090. The only additional line required is one programmable output pin (C0) to control $\overline{CS}$ on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

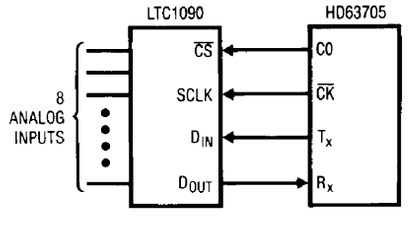

Figure 1. Schematic

Hardware Description

The 63705 was emulated and the code for this interface was developed on a Hitachi H35MIX3 emulator.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. ACLK of the LTC1090 was 2 MHz and the 63705 clock was 4 MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

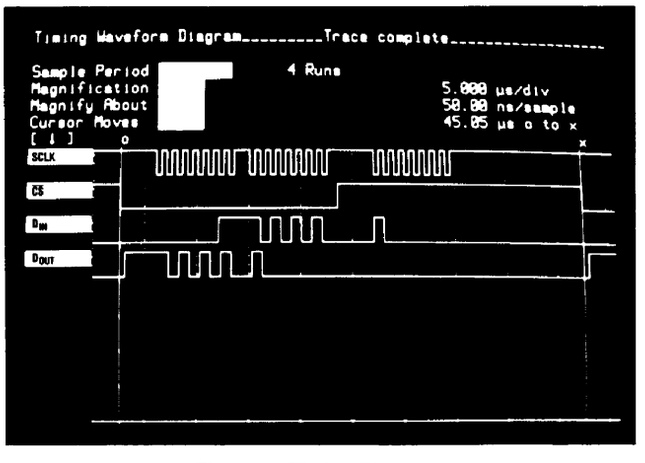

Figure 2. Timing Diagram

Software Description

The software configures and controls the SCI of the 63705. Additionally, the software manipulates C0 ($\overline{CS}$ of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

The code first configures the SCI control register (SCR). D3 and D4 are set as the SCI output and input respectively. D5 is selected as a clock output with a frequency one fourth the crystal frequency. Next, the SCI status register (SSR) is configured so that the interrupts are disabled. Data is transmitted on the falling edge of the clock and received on the rising edge of the clock.

Port C is configured as all outputs by setting the data direction register (address $06). A D_{IN} word that configures the LTC1090 for CH0 with respect to CH1, bipolar, LSB first and a 16-bit word length is stored in $50. Figure 3 shows how the D_{IN} word is composed. Note, that for LSB first format the D_{IN} word must be constructed opposite from MSB first format. This is so that each bit of the D_{IN} word is always shifted into the LTC1090 in the same order.

C0 is made to go low. D_{IN} for the LTC1090 is loaded into the SCI data register (SDR). Storing D_{IN} in the SDR causes the transfer to begin. After waiting for the first eight bits to be transferred (6 NOPs) the data containing the LSBs from the LTC1090 is loaded into the accumulator and then stored in $61 of the 63705 RAM. The act of reading the LSBs into the ACC causes the next SCI transfer to begin. C0 is set and the MSBs from the LTC1090 are loaded into the ACC and then stored in $62 of the 63705 RAM.

1	1	0	0	0	0	0	0	
WL0	WL1	MSBF	UNI	S2	S1	O/S	S/D	$50

Figure 3. D_{IN} Word for LTC1090 Stored in 63705 RAM

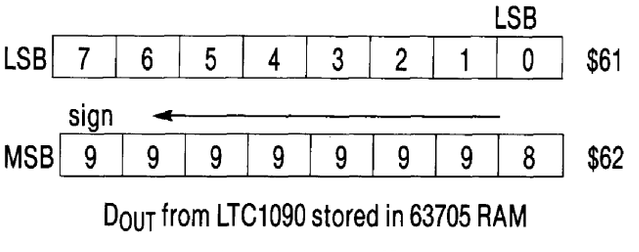

Figure 4. Memory Map

LABEL	MNEMONIC		COMMENTS
	LDA	#$E0	CONFIGURATION DATA FOR SCR
	STA	$10	LOAD DATA INTO SCR ($10)
	LDA	#$30	CONFIGURATION DATA FOR SSR
	STA	$11	LOAD DATA INTO SSR ($11)
	LDA	#$FF	CONFIG. DATA FOR PORT C DDR
	STA	$06	LOAD DATA INTO PORT C DDR
	LDA	#$C0	LOAD LTC1090 D_{IN} DATA INTO ACC
	STA	$50	LOAD LTC1090 D_{IN} DATA INTO $50
START	LDA	$50	LOAD D_{IN} INTO ACC FROM $50
	BCLR	0,$02	C0 GOES LOW ($\overline{CS}$ GOES LOW)
	STA	$12	LOAD D_{IN} INTO SDR. START SCK
	NOP		6 NOPs FOR TIMING
	LDA	$12	LOAD LSBs. START NEXT CYCLE
	STA	$61	STORE LSBs IN $61
	NOP		1 NOP FOR TIMING
	BSET	0,$02	C0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDA	$12	LOAD MSBs
	STA	$62	STORE MSBs IN $62

Figure 5. 63705 Code

The data at this point is right justified with the sign bit (B9) being extended into B1-B7 of $62 as shown in Figure 4.

At this time 44 ACLK cycles must be allowed for the A/D to perform its next conversion. Usually the processor will have other tasks to perform during this time (you have to do something with the data once the processor has it). If this is not the case, a string of NOPs or a simple delay loop can be used to generate this delay.

Summary

A four wire interface between the LTC1090 and the Hitachi 63705 with a combined data conversion and transfer time of 45μs was demonstrated. The interface used the serial (SCI) port of the 63705. Because the SCI port transfers data LSB first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1090. The 10 data bits of the LTC1090 are shifted LSB first in two eight bit transfers. The data is stored right justified in the 63705s internal RAM.